

AMERICAN  
TECHNICAL  
CERAMICS

## LTCC PRODUCTS



 ENGINEERS'  
CHOICE™

Design Guidelines for LTCC Multilayer Circuits,  
Modules, Packages & Components

## LTCC Technology

Low Temperature Co-fired Ceramics (LTCC) is an enabling technology, now recognized globally as one of the most advanced and valuable solutions for the miniaturization of electronics packaging. In both military and commercial applications, lower weight and smaller size requirements necessitate increasing density in electronics packaging.

LTCC is used to create three-dimensional circuits, bringing together passive elements and semi-conductor components into one high density and highly versatile electronic module. Co-fired Ceramic Product (CCP) technology is ideally suited to modular applications requiring high circuit density, high operating temperature and high power dissipation, for low cost high volume manufacturing.

## Turn Key Production Capabilities

ATC's CCP division is a world-class producer of ceramic packages. We have the ability to produce a variety of LTCC substrates, packages and structures from engineering prototypes to MIL-STD-883 compliant hardware. ATC offers extensive expertise using standard ceramic tapes such as Ferro and Du-Pont as well as our own ATC tape system. Our on-site capabilities include:

- Board sizes up to 5.5" x 5.5" with simple or complex part shapes
- Auto alignment and 100% inspection
- Up to 40 tape layers achievable
- Buried and surface resistors
- Surface thin film metalization
- Co-fired and post-fired solderable metal outer layers
- Design, assembly and test services

## Advanced Material Abilities

At ATC's CCP division we pride ourselves in customizing ceramic tape for high volume product applications. ATC has more than 40 years experience in formulating ceramic tape and electrode ink systems. The Company is unique for its full time materials research and development team, capable of meeting the most challenging requirements. The CCP division has successfully manufactured products using combinations of tape with diverse dielectric constants. We satisfy the needs of engineers seeking:

- Superior reliability
- Multiple component modules
- Low developmental costs
- High density packaging
- High volume manufacturing
- Consistent high quality
- A robust solution
- Laser cutting for complex shapes
- Braze Au/Sn and Au/Ge

## ATC'S Focus on Quality

Quality is the hallmark of every product shipped by ATC. ATC is ISO 9001:2000 registered. ATC's CCP Division utilizes process control and continuous improvement methodologies to ensure reliable product quality.



Baccini automated printer and punch system for better accuracy and efficiency



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# ATC CCP DESIGN GUIDELINES

The guidelines on this page should not limit the complexity or ingenuity of designs. Each design will be reviewed with respect to manufacturing robustness, manufacturing cycle times, cost and reliability.

## Ceramic Systems

Specifications	*ATC	Dupont 951	Dupont 943	Ferro A6M	Ferro A6S	Heraeus CT2000
<b>Electrical Properties</b>						
Dielectric Constant	5.9	7.8	7.5	5.9	5.9	9.1
Dissipation Factor @ 1MHz (Max.)	<2 x 10 <sup>-3</sup>	<4.5 x 10 <sup>-3</sup>	<1 x 10 <sup>-3</sup>	<2 x 10 <sup>-3</sup>	<2 x 10 <sup>-3</sup>	<2 x 10 <sup>-3</sup>
Breakdown Voltage (v/mil)	>800	>1000	>1000	>800	>800	—
Insulation Resistance @100 vdc (ohms)	>10 <sup>12</sup>	>10 <sup>12</sup>	>10 <sup>12</sup>	>10 <sup>12</sup>	>10 <sup>12</sup>	>10 <sup>13</sup>
<b>Dimensional Characteristics</b>						
Tape layer Thickness - Green - (mils)	4.0 to 10	2.0, 4.5, 6.5, 10	2.0, 5.0, 10.0	5.0, 10	5.0, 10	2.0, 3.9
Tape layer Thickness - Fired - (mils)	3.6 to 8.0	1.7, 3.8, 5.5, 8.5	1.8, 4.5, 9.0	3.7, 7.4	3.9, 7.7	1.8, 3.5
**Shrinkage x, y (%) ± 0.3	12.0	13.0	9.5	15.2	16	11.5
**Shrinkage z (%) ± 0.5	20	15.0	10.3	26	23	14
Surface Finished as Fired (microinches)	<15	<10	<25	<10	<10	<10
Camber (mils/in.)	<2	<2	<2	<2	<2	<4
Color	white	blue	lt. blue	white	white	blue
<b>Thermal Properties</b>						
TCE 25°C to 300°C (ppm/°C)	8.6	5.8	6.0	7.0	9.0	8.5
Thermal Conductivity (W/m °K)	1.6	3.0	4.4	2.0	2.0	4.3
<b>Mechanical Properties</b>						
Density (gm/cm <sup>3</sup> )	4.46	3.10	3.20	2.45	2.45	3.05
Flexural Strength (Mpa)	>170	320	230	>170	>160	310
Youngs Modulus (Gpa)	—	152	149	92	82	—
Shear Modulus (Gpa)	—	—	—	32	—	—
Poissons Ratio	—	0.17	0.25	0.26	0.26	—

## Typical Metal Properties

Circuit Type	Resistivity (mV / sq.)	Dry Thickness (μm)
Ag circuits	1 - 5	8 - 15
Au circuits	3 - 5	8 - 15
Au via fill	5 - 15	N/A
Ag via fill	2 - 3	N/A
Sn - Pb Solderable	30 - 50	15 - 35
Au-Sn, Au-Ge, Bi-Sn, In-Pb	<5	25 - 40

## Package Dimensions

Maximum Size (Inches)	Minimum Size (Inches)	Minimum Thickness (Inches)	Maximum Thickness (Inches)
5.5 x 5.5	0.025 x 0.025	0.010	0.250

\* In Development; please consult ATC for the most current technical information.

\*\* Shrinkage numbers are for reference only and may vary based on design factors such as metal loading.



Baccini automated printer and collator system with layer to layer accuracy of ± 0.0005"

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## Ground/Power Planes

Planes should be a grid with a minimum 10 mil line and space pattern. Each plane shall be offset or a different grid angle pattern from the previous pattern. Partial plane coverage of less than 75% of the designed substrate area is not recommended due to irregular fired shrinkage. The internal plane perimeters shall be staggered in and out same distance as the line widths used in the grid pattern. The external plane may be a solid pattern.

## Brazing

The brazing area is made up of an adhesive and barrier layer. The first conductor pattern (the adhesive layer) shall be 2 mil larger in width and 1 mil larger in length than the barrier pattern.

## Seal Ring

The nominal brazing conductor pattern shall be 20 mils wider than the nominal seal ring width with outside corner square and inside corner radius 20 mil less than the nominal inside seal ring radius.

## Resistors

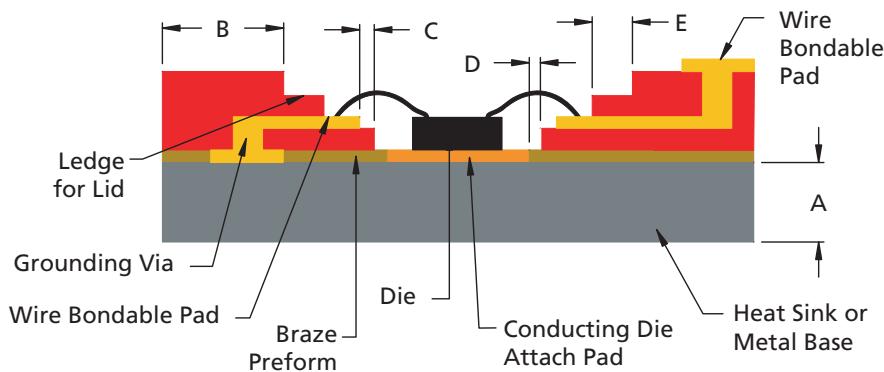
The minimum resistor size shall be 30 mils by 30 mils, with a minimum 5 mils overlap of the resistor to the conductor. All resistors shall be designed with an aspect ratio of 75% of the nominal value (100% for buried resistors). Aspect ratio is defined as  $R=R_s(L/W)$ , where R is resistor value,  $R_s$  is sheet resistivity, L is the length of the resistor and W is the width of the resistor.

The minimum resistor laser probe pad size shall be 15 mils square. Resistors shall be designed using the following sheet resistivities:

**Ohms/Square: (Post fired Dupont 951 only):** 50 to 1M; **Co-Fired Du Pont 951 and Co-fired Ferro A6:** 10 to 10K

## Cavity Construction

Cavities are formed by removing the material in the unfired (green) ceramic tape or by laser cutting. To reduce the possibility of exposed metal on cavity walls the metallization shall be pulled back from the edge of the cavity. If the cavity of the floor is fully metallized, the metallization should extend beyond the cavity walls to ensure complete coverage. For volume production the most cost effective method for cavity formation is a tool and die punch. Dedicated tooling can be purchased for large volume orders to reduce time and cost of cavity formation. The diagram below explains cavity design guidelines.



## Cavity Features

Features	Location	Standard (Inches)	Premium (inches)
Distance between edge of the wire bond pad & cavity edge (Min.)	C	>0.004	0.002
Internal Metallization Pull back from the edge of cavity (Min.)	—	>0.010	0.006
Distance between outside corner of the ledge and the edge of the substrate (Min.)	D	>0.125	0.030
Ceramic Ledge width for lid (Min.)	B	>0.025	0.015*
Cavity corner radius (Typ.)	E	0.025	0.015
Cavity Dimension Tolerance (Min.)	—	> +/-1% or +/-0.005	+/-0.003
Heat sink/base metal thickness	A	N/A	N/A

\*While designing ledge take into consideration any future assembly needs: wire bonding, solder attach, etc.

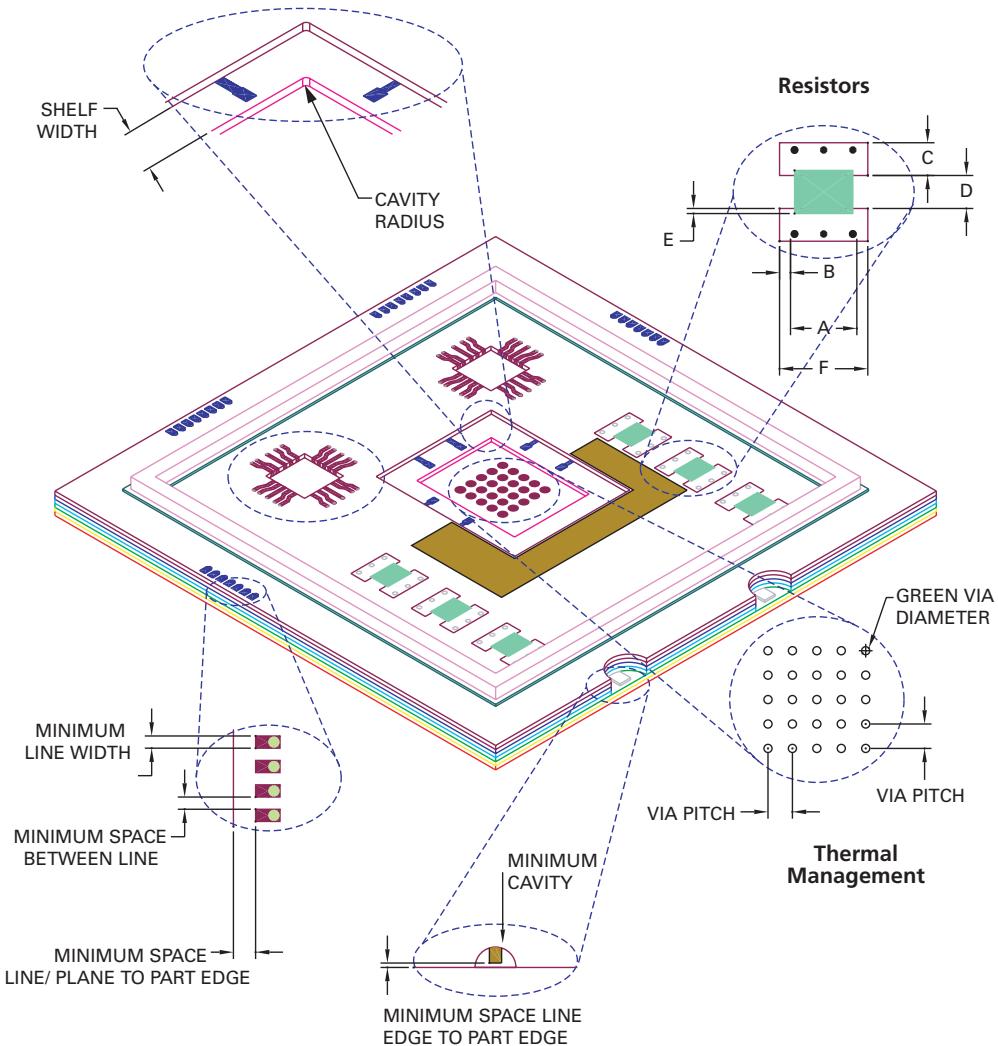
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## Circuit Features



## Vias

Stacked vias create a thermal and electrical connection between sources such as a semiconductor die to the metal base. The thermal conductivity (TC) of a typical array of electrical conducting 0.008" diameter vias on a 0.024" pitch is approximately 54 W/m/C. The thermal performance of the package can be enhanced by either adding an array of thermal vias described above or replacing the ceramic base with a brazed heat sink such as molybdenum, copper tungsten (Cu-W) or copper-moly-copper (Cu-Mo-Cu).

The vias are punched in the green stage, and the recommended aspect ratio is 1:1 with the via diameter close to tape thickness (e.g. 6 mil via in 5 mil tape). In cases where hermeticity is required, the vias should be staggered between tape layers at two times the diameter. The vias can be stacked between any number of layers but each via should have a catch pad extending at least 2 mil from the edge of the via. Vias are composed of glass and metal that expands and contracts at a greater rate than the surrounding ceramics. As a result, a posting effect may occur, where the via may project above each tape layer by as much as 2 mil., creating distortion of features such as lines, spaces, and components that are adjacent to the stacked vias. The result can be reduced by staggering vias.

It is recommended that vias should not be placed directly under solderable areas as the glass in the via fill material may migrate to the surface of the SMT region. This can result in solder dewetting around the vias.

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## Guidelines for Circuit Features

Features – As Fired	Standard	Premium
<b>Printed Circuits:</b>		
Minimum Line Width (Inches)	0.005	0.003
Minimum Space Between Lines (Inches)	0.005	0.004
Minimum Space Line-to-Part Edge (Inches)	0.010	0.006
Line Width Tolerance (Inches)	$\pm 0.001$	$\pm 0.0005$
Line Space Tolerance (Inches)	$\pm 0.001$	$\pm 0.0005$
<b>Ground/Power Planes:</b>		
Minimum Grid Line/Space (Inches)	0.015/0.015	0.010/0.010 or Solid (External only)
Minimum Space, Plane-to-Line (Inches)	0.010	0.006
Maximum Percent Coverage	50	100
<b>Vias:</b>		
Green Via Diameter (Mils)*	6, 8, 10, 12	4
Via Pitch	3 x diameter	2.0 x diameter
Min. Distance Via Edge to Part Edge (Inches)	0.010	0 (Castellations)
Maximum Layers with Stacked Vias (before stagger)**	8	25
Min. Distance Via or Cover Pad Edge to Conductor Track (Inches)	0.008	0.005
Thermal Slots (Inches)	None, via array is preferred	<0.010 wide, <0.040 long
Via Layer-to-Layer Alignment Tolerance (Inches)***	$\pm 0.002$	N/A
Fired Via Diameter Tolerance (Inches)	$\pm 0.0005$	N/A
Via-to-Via Location Tolerance (Inches)	$\pm 0.001$	N/A
Conductor extension beyond resistor width "B" (Inches, Min.)	0.020	0.005
<b>Resistors:</b>		
Resistor Tolerance As fired (Min. %)	30	Trim to Value (Surface)
Resistor Width "A" (Inches, Min.)	0.070	0.030
Conductor extension beyond width "B" (Inches, Min.)	0.020	0.005
Conductor length "C" (Inches, Min.)	0.060	0.030
Effective resistor length "D" (Inches, Min.)	0.070	0.030
Conductor overlap of the resistor "E" (Inches, Min.)	0.020	0.010
Overall conductor width "F" ( C + 10 Inches, Min.)	0.090	0.040

\* Fired via diameters are typically 5-15% smaller than the green diameters, depending on the material.

\*\* Staggered vias must be used for hermetic packaging.

\*\*\* Via and conductor tolerances are designed to meet shielding requirements.

NOTE: Redundant vias are preferred where possible to reduce the opportunity for open circuits. Circuit widths should overlap vias entirely. Cover pads are preferred on all vias in hermetic packages.



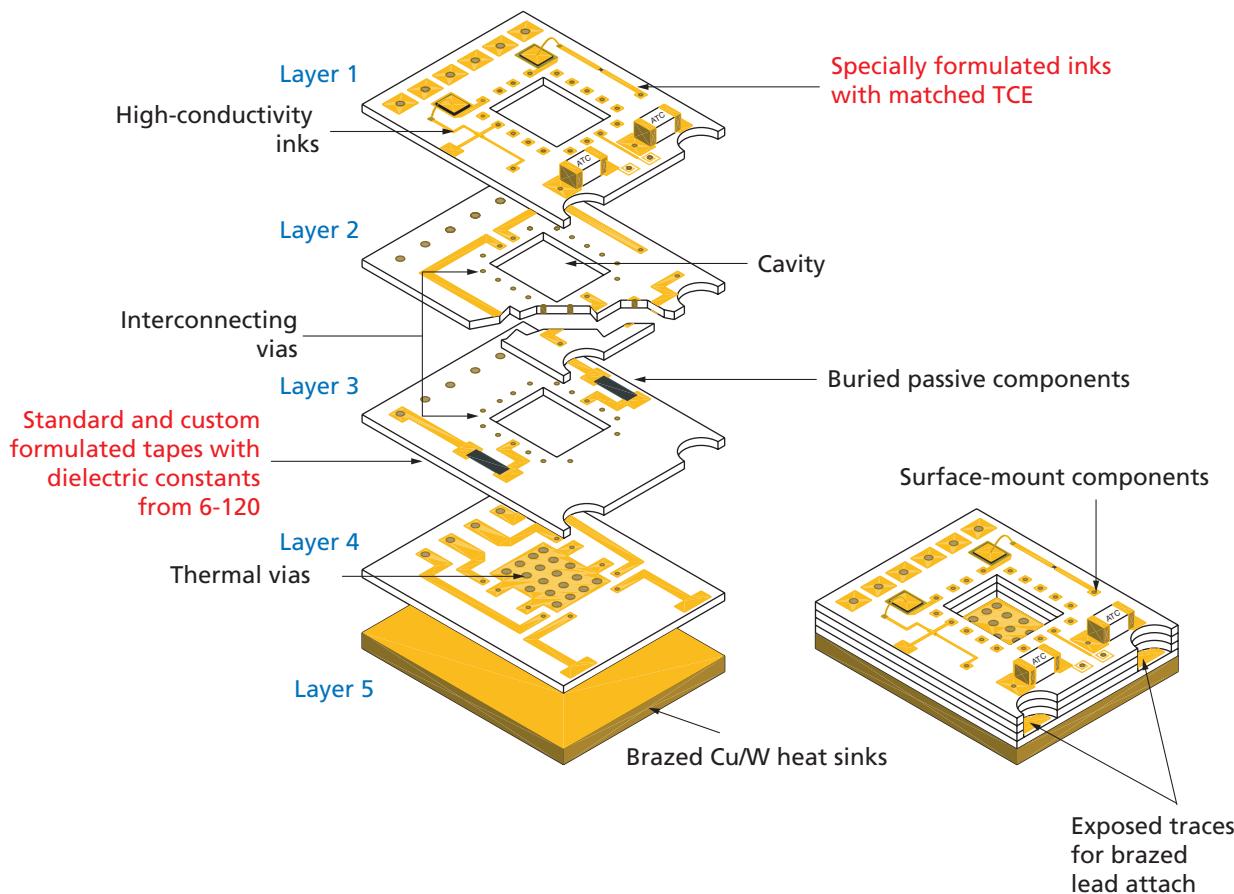
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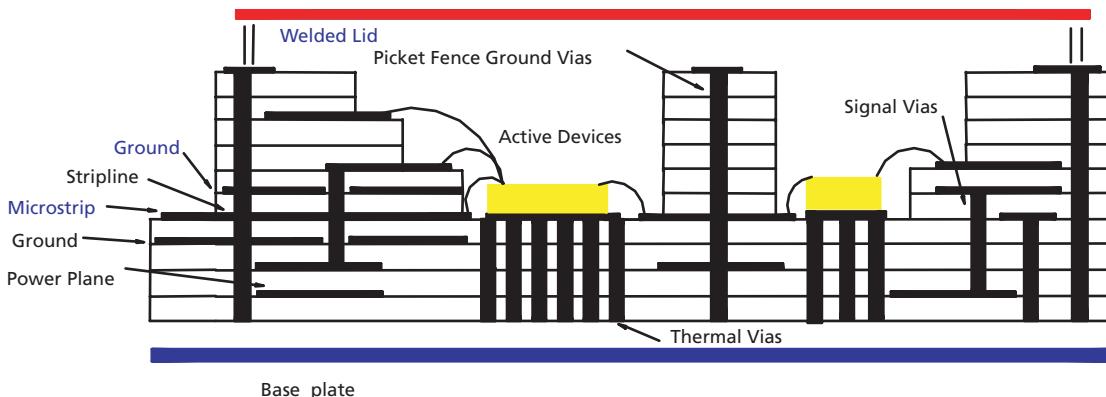
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## Available Product Features



## Typical LTCC Architecture



## The ATC Advantage

- Limited production runs to support engineering prototypes
- ATC can apply a variety of processes to achieve required tolerances
- ATC maintains complete process control through all phases of manufacturing

- Serialization for traceability
- Fully qualified electrode inks assure consistent performance
- ATC can provide many finishing services to deliver ready-to-use parts

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## Design Data Format

The preferred design data formats are

- AutoCAD – DWG
- Gerber RS-274X  
(embedded apertures)

Alternative Formats

- DXF
- RS-274 with complete aperture list

Design data should be in single image, final dimension format.

## Vias

- Vias should be flashes, not drawn

## Cavities

- Cavities should be specified by closed polylines having 0.001" line width

## Circuits

- Circuits may be draws or filled polylines

## Customer Should Supply

- Data files (Gerber)
- Drawing (DXF, DWG, Gerber)
- Assembly drawing (if applicable)
- Circuit test net list
- Acceptance criteria (mil std, process spec, etc.)
- Layup - stacking order of each print and via

## ATC is your one stop shop for your 3-D, high-performance requirements



- Custom-tailored tape
- Cost-effective approach with buried passive components
- TCE matched, high-conductivity ink systems
- Specially formulated thermal via ink
- Fine line geometry using a variety of processes

*Integration of the Best Attributes of Thick Film, Thin Film,  
LTCC and HTCC Technologies*

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